

t15_memstr_0 (TMTH- fJVq4fv3JmJmPwZhUJEqcEdC7hwJZzd)

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Let $v1_setfam_1 : \iota \Rightarrow o$ be given. Let $v2_struct_0 : \iota \Rightarrow o$ be given. Let $v2_memstr_0 : \iota \Rightarrow \iota \Rightarrow o$ be given. Let $v3_memstr_0 : \iota \Rightarrow \iota \Rightarrow o$ be given. Let $l1_memstr_0 : \iota \Rightarrow \iota \Rightarrow o$ be given. Let $v7_ordinal1 : \iota \Rightarrow o$ be given. Let $k4_struct_0 : \iota \Rightarrow \iota$ be given. Let $k9_xtuple_0 : \iota \Rightarrow \iota$ be given. Let $k7_memstr_0 : \iota \Rightarrow \iota \Rightarrow \iota \Rightarrow \iota$ be given. Let $v1_xboole_0 : \iota \Rightarrow o$ be given. Let $v1_relat_1 : \iota \Rightarrow o$ be given. Let $v4_relat_1 : \iota \Rightarrow \iota \Rightarrow o$ be given. Let $u1_struct_0 : \iota \Rightarrow \iota$ be given. Let $v1_funct_1 : \iota \Rightarrow o$ be given. Let $v5_funct_1 : \iota \Rightarrow \iota \Rightarrow o$ be given. Let $k2_memstr_0 : \iota \Rightarrow \iota \Rightarrow \iota$ be given. Let $v5_memstr_0 : \iota \Rightarrow \iota \Rightarrow \iota \Rightarrow \iota \Rightarrow o$ be given. Let $k5_memstr_0 : \iota \Rightarrow \iota \Rightarrow \iota \Rightarrow \iota$ be given. Assume the following.

$$\begin{aligned} & \forall X0. \forall X1. \forall X2. ((\neg v1_setfam_1 X0) \wedge (((\neg v2_struct_0 \\ & X1) \wedge ((v2_memstr_0 X1 X0) \wedge ((v3_memstr_0 X1 X0) \wedge (l1_memstr_0 X1 \\ & X0)))) \wedge (v7_ordinal1 X2))) \Rightarrow ((\neg v1_xboole_0 (k7_memstr_0 X0 X1 \\ & X2)) \wedge ((v1_relat_1 (k7_memstr_0 X0 X1 X2)) \wedge ((v4_relat_1 (k7_memstr_0 \\ & X0 X1 X2) (u1_struct_0 X1)) \wedge ((v1_funct_1 (k7_memstr_0 X0 X1 X2)) \wedge \\ & ((v5_funct_1 (k7_memstr_0 X0 X1 X2) (k2_memstr_0 X0 X1)) \wedge (v5_memstr_0 \\ & (k7_memstr_0 X0 X1 X2) X0 X1 X2)))))) \end{aligned} \tag{1}$$

Assume the following.

$$\begin{aligned} & \forall X0. (\neg v1_setfam_1 X0) \Rightarrow (\forall X1. ((\neg v2_struct_0 X1) \wedge \\ & ((v2_memstr_0 X1 X0) \wedge ((v3_memstr_0 X1 X0) \wedge (l1_memstr_0 X1 X0)))) \Rightarrow \\ & (\forall X2. (v7_ordinal1 X2) \Rightarrow (\forall X3. ((v1_relat_1 X3) \wedge (\\ & (v4_relat_1 X3 (u1_struct_0 X1)) \wedge ((v1_funct_1 X3) \wedge (v5_funct_1 \\ & X3 (k2_memstr_0 X0 X1)))) \Rightarrow ((v5_memstr_0 X3 X0 X1 X2) \Leftrightarrow ((k4_struct_0 \\ & X1 \in k9_xtuple_0 X3) \wedge (k5_memstr_0 X0 X1 X3 = X2)))))) \end{aligned} \tag{2}$$

Theorem 1

$$\begin{aligned} & \forall X0. (\neg v1_setfam_1 X0) \Rightarrow (\forall X1. ((\neg v2_struct_0 X1) \wedge \\ & ((v2_memstr_0 X1 X0) \wedge ((v3_memstr_0 X1 X0) \wedge (l1_memstr_0 X1 X0)))) \Rightarrow \\ & (\forall X2. (v7_ordinal1 X2) \Rightarrow (k4_struct_0 X1 \in k9_xtuple_0 (k7_memstr_0 \\ & X0 X1 X2))) \end{aligned}$$