

t1_gate_4 (TMVQaZasEKvBbjd- mYM5fPvb744WiNeviTrT)

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Let $v1_xboole_0 : \iota \Rightarrow o$ be given. Let $k4_gate_1 : \iota \Rightarrow \iota \Rightarrow \iota$ be given. Let $k2_gate_1 : \iota \Rightarrow \iota \Rightarrow \iota$ be given. Assume the following.

$$\forall X0. \forall X1. ((\neg v1_xboole_0 X0) \wedge (\neg v1_xboole_0 X1)) \Rightarrow (v1_xboole_0 (k4_gate_1 X0 X1)) \quad (1)$$

Assume the following.

$$\forall X0. \forall X1. ((v1_xboole_0 X0) \wedge (v1_xboole_0 X1)) \Rightarrow (v1_xboole_0 (k4_gate_1 X0 X1)) \quad (2)$$

Assume the following.

$$\forall X0. \forall X1. ((v1_xboole_0 X0) \wedge (\neg v1_xboole_0 X1)) \Rightarrow (\neg v1_xboole_0 (k4_gate_1 X0 X1)) \quad (3)$$

Assume the following.

$$\forall X0. \forall X1. (v1_xboole_0 X0) \Rightarrow (v1_xboole_0 (k2_gate_1 X0 X1)) \quad (4)$$

Assume the following.

$$\forall X0. \forall X1. ((\neg v1_xboole_0 X0) \wedge (\neg v1_xboole_0 X1)) \Rightarrow (\neg v1_xboole_0 (k2_gate_1 X0 X1)) \quad (5)$$

Assume the following.

$$\forall X0. \forall X1. k4_gate_1 X0 X1 = k4_gate_1 X1 X0 \quad (6)$$

Assume the following.

$$\forall X0. \forall X1. k2_gate_1 X0 X1 = k2_gate_1 X1 X0 \quad (7)$$

Theorem 1

$$\begin{aligned} & \forall X0.\forall X1.\forall X2.\forall X3.\forall X4.\forall X5. \\ & \forall X6.\forall X7.\forall X8.\forall X9.\forall X10.\forall X11. \\ & \forall X12.\forall X13.\forall X14.\forall X15.\forall X16. \\ & \forall X17.\forall X18.\forall X19.\forall X20.\forall X21. \\ & \forall X22.\forall X23.\forall X24.\forall X25.\forall X26. \\ & \forall X27.\forall X28.\forall X29.\forall X30.\forall X31. \\ & \forall X32.\forall X33.\forall X34.\forall X35.\forall X36. \\ & \forall X37.\neg(\neg v1_xboole_0 X12)\wedge((\neg(\neg v1_xboole_0 X25)\wedge(v1_xboole_0 \\ & (k4_gate_1 X37 (k2_gate_1 X0 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 \\ & X37 (k2_gate_1 X0 X24)))\wedge(v1_xboole_0 X25))\wedge((\neg(\neg v1_xboole_0 \\ & X26)\wedge(v1_xboole_0 (k4_gate_1 X13 (k2_gate_1 X1 X24))))\wedge((\neg(\neg \\ & v1_xboole_0 (k4_gate_1 X13 (k2_gate_1 X1 X24)))\wedge(v1_xboole_0 \\ & X26))\wedge((\neg(\neg v1_xboole_0 X27)\wedge(v1_xboole_0 (k4_gate_1 X14 (k2_gate_1 \\ & X2 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 X14 (k2_gate_1 X2 X24)))\wedge \\ & (v1_xboole_0 X27))\wedge((\neg(\neg v1_xboole_0 X28)\wedge(v1_xboole_0 (k4_gate_1 \\ & X15 (k2_gate_1 X3 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 X15 (k2_gate_1 \\ & X3 X24)))\wedge(v1_xboole_0 X28))\wedge((\neg(\neg v1_xboole_0 X29)\wedge(v1_xboole_0 \\ & (k4_gate_1 X16 (k2_gate_1 X4 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 \\ & X16 (k2_gate_1 X4 X24)))\wedge(v1_xboole_0 X29))\wedge((\neg(\neg v1_xboole_0 \\ & X30)\wedge(v1_xboole_0 (k4_gate_1 X17 (k2_gate_1 X5 X24))))\wedge((\neg(\neg \\ & v1_xboole_0 (k4_gate_1 X17 (k2_gate_1 X5 X24)))\wedge(v1_xboole_0 \\ & X30))\wedge((\neg(\neg v1_xboole_0 X31)\wedge(v1_xboole_0 (k4_gate_1 X18 (k2_gate_1 \\ & X6 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 X18 (k2_gate_1 X6 X24)))\wedge \\ & (v1_xboole_0 X31))\wedge((\neg(\neg v1_xboole_0 X32)\wedge(v1_xboole_0 (k4_gate_1 \\ & X19 (k2_gate_1 X7 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 X19 (k2_gate_1 \\ & X7 X24)))\wedge(v1_xboole_0 X32))\wedge((\neg(\neg v1_xboole_0 X33)\wedge(v1_xboole_0 \\ & (k4_gate_1 X20 (k2_gate_1 X8 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 \\ & X20 (k2_gate_1 X8 X24)))\wedge(v1_xboole_0 X33))\wedge((\neg(\neg v1_xboole_0 \\ & X34)\wedge(v1_xboole_0 (k4_gate_1 X21 (k2_gate_1 X9 X24))))\wedge((\neg(\neg \\ & v1_xboole_0 (k4_gate_1 X21 (k2_gate_1 X9 X24)))\wedge(v1_xboole_0 \\ & X34))\wedge((\neg(\neg v1_xboole_0 X35)\wedge(v1_xboole_0 (k4_gate_1 X22 (k2_gate_1 \\ & X10 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 X22 (k2_gate_1 X10 X24)))\wedge \\ & (v1_xboole_0 X35))\wedge((\neg(\neg v1_xboole_0 X36)\wedge(v1_xboole_0 (k4_gate_1 \\ & X23 (k2_gate_1 X11 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 X23 (k2_gate_1 \\ & X11 X24)))\wedge(v1_xboole_0 X36))\wedge((\neg(\neg v1_xboole_0 X24)\wedge(v1_xboole_0 \\ & (k2_gate_1 X12 X24))))\wedge((\neg(\neg v1_xboole_0 (k2_gate_1 X12 X24))\wedge \\ & (v1_xboole_0 X24))\wedge((\neg(\neg v1_xboole_0 X23)\wedge(v1_xboole_0 (k4_gate_1 \\ & X36 (k2_gate_1 X11 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 X36 (k2_gate_1 \\ & X11 X24)))\wedge(v1_xboole_0 X23))\wedge((\neg(\neg v1_xboole_0 X22)\wedge(v1_xboole_0 \\ & (k4_gate_1 X35 (k2_gate_1 X10 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 \\ & X35 (k2_gate_1 X10 X24)))\wedge(v1_xboole_0 X22))\wedge((\neg(\neg v1_xboole_0 \\ & X21)\wedge(v1_xboole_0 (k4_gate_1 X34 (k2_gate_1 X9 X24))))\wedge((\neg(\neg \\ & v1_xboole_0 (k4_gate_1 X34 (k2_gate_1 X9 X24)))\wedge(v1_xboole_0 \\ & X21))\wedge((\neg(\neg v1_xboole_0 X20)\wedge(v1_xboole_0 (k4_gate_1 X33 (k2_gate_1 \\ & X8 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 X33 (k2_gate_1 X8 X24)))\wedge \\ & (v1_xboole_0 X20))\wedge((\neg(\neg v1_xboole_0 X19)\wedge(v1_xboole_0 (k4_gate_1 \\ & X32 (k2_gate_1 X7 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 X32 (k2_gate_1 \\ & X7 X24)))\wedge(v1_xboole_0 X19))\wedge((\neg(\neg v1_xboole_0 X18)\wedge(v1_xboole_0 \\ & (k4_gate_1 X31 (k2_gate_1 X6 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 \\ & X31 (k2_gate_1 X6 X24)))\wedge(v1_xboole_0 X18))\wedge((\neg(\neg v1_xboole_0 \\ & X17)\wedge(v1_xboole_0 (k4_gate_1 X30 (k2_gate_1 X5 X24))))\wedge((\neg(\neg \\ & v1_xboole_0 (k4_gate_1 X30 (k2_gate_1 X5 X24)))\wedge(v1_xboole_0 \\ & X17))\wedge((\neg(\neg v1_xboole_0 X16)\wedge(v1_xboole_0 (k4_gate_1 X29 (k2_gate_1 \\ & X4 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 X29 (k2_gate_1 X4 X24)))\wedge \\ & (v1_xboole_0 X16))\wedge((\neg(\neg v1_xboole_0 X15)\wedge(v1_xboole_0 (k4_gate_1 \\ & X28 (k2_gate_1 X3 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 X28 (k2_gate_1 \\ & X3 X24)))\wedge(v1_xboole_0 X15))\wedge((\neg(\neg v1_xboole_0 X14)\wedge(v1_xboole_0 \\ & (k4_gate_1 X27 (k2_gate_1 X2 X24))))\wedge((\neg(\neg v1_xboole_0 (k4_gate_1 \\ & X27 (k2_gate_1 X2 X24)))\wedge(v1_xboole_0 X14))\wedge((\neg(\neg v1_xboole_0 \end{aligned}$$