

t4_gate_2
(TMbC3yKwfNeSJBRCk9wNgcaQ1KMTcmM1cXD)

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Let $v1_xboole_0 : \iota \Rightarrow o$ be given. Let $k8_gate_1 : \iota \Rightarrow \iota \Rightarrow \iota \Rightarrow \iota$ be given. Let $k1_gate_1 : \iota \Rightarrow \iota$ be given. Let $k2_gate_1 : \iota \Rightarrow \iota \Rightarrow \iota$ be given. Let $k4_gate_1 : \iota \Rightarrow \iota \Rightarrow \iota$ be given. Let $k3_gate_1 : \iota \Rightarrow \iota \Rightarrow \iota$ be given. Assume the following.

$$\begin{aligned} \forall X0. \forall X1. (&\neg(\neg v1_xboole_0 (k4_gate_1 X0 X1)) \wedge ((\neg \\ &(\neg v1_xboole_0 X0) \wedge (v1_xboole_0 X1)) \wedge (\neg(v1_xboole_0 X0) \wedge (\neg v1_xboole_0 \\ &X1)))) \wedge (\neg(((\neg v1_xboole_0 X0) \wedge (v1_xboole_0 X1)) \vee ((v1_xboole_0 \\ &X0) \wedge (\neg v1_xboole_0 X1)))) \wedge (v1_xboole_0 (k4_gate_1 X0 X1))) \end{aligned} \quad (1)$$

Assume the following.

$$\begin{aligned} \forall X0. \forall X1. (&\neg(\neg v1_xboole_0 (k3_gate_1 X0 X1)) \wedge ((v1_xboole_0 \\ &X0) \wedge (v1_xboole_0 X1))) \wedge (\neg(\neg(v1_xboole_0 X0) \wedge (v1_xboole_0 X1)) \wedge \\ &(v1_xboole_0 (k3_gate_1 X0 X1))) \end{aligned} \quad (2)$$

Assume the following.

$$\forall X0. \forall X1. (\neg v1_xboole_0 (k2_gate_1 X0 X1)) \Leftrightarrow ((\neg v1_xboole_0 X0) \wedge (\neg v1_xboole_0 X1)) \quad (3)$$

Assume the following.

$$\forall X0. \forall X1. (\neg v1_xboole_0 X1) \Rightarrow (\neg v1_xboole_0 (k3_gate_1 X0 X1)) \quad (4)$$

Assume the following.

$$\forall X0. \forall X1. (v1_xboole_0 X0) \Rightarrow (v1_xboole_0 (k2_gate_1 X0 X1)) \quad (5)$$

Assume the following.

$$\forall X0. \forall X1. ((\neg v1_xboole_0 X0) \wedge (\neg v1_xboole_0 X1)) \Rightarrow (\neg v1_xboole_0 (k2_gate_1 X0 X1)) \quad (6)$$

Assume the following.

$$\forall X0.(\neg v1_xboole_0 X0)\Rightarrow(v1_xboole_0 (k1_gate_1 X0)) \quad (7)$$

Assume the following.

$$\forall X0.\forall X1.\forall X2.(v1_xboole_0 X0)\Rightarrow(v1_xboole_0 (k8_gate_1 X1 X2 X0)) \quad (8)$$

Assume the following.

$$\forall X0.(v1_xboole_0 X0)\Rightarrow(\neg v1_xboole_0 (k1_gate_1 X0)) \quad (9)$$

Assume the following.

$$\forall X0.\forall X1.\forall X2.(v1_xboole_0 X0)\Rightarrow(v1_xboole_0 (k8_gate_1 X1 X0 X2)) \quad (10)$$

Assume the following.

$$\forall X0.\forall X1.\forall X2.(v1_xboole_0 X0)\Rightarrow(v1_xboole_0 (k8_gate_1 X0 X1 X2)) \quad (11)$$

Assume the following.

$$\forall X0.\forall X1.\forall X2.((\neg v1_xboole_0 X0)\wedge((\neg v1_xboole_0 X1)\wedge(\neg v1_xboole_0 X2)))\Rightarrow(\neg v1_xboole_0 (k8_gate_1 X0 X1 X2)) \quad (12)$$

Assume the following.

$$\forall X0.\forall X1.k4_gate_1 X0 X1 = k4_gate_1 X1 X0 \quad (13)$$

Assume the following.

$$\forall X0.\forall X1.k2_gate_1 X0 X1 = k2_gate_1 X1 X0 \quad (14)$$

Theorem 1

$$\begin{aligned}
& \forall X0. \forall X1. \forall X2. \forall X3. \forall X4. \forall X5. \\
& \forall X6. \forall X7. \forall X8. \forall X9. \forall X10. \forall X11. \\
& \forall X12. \forall X13. \forall X14. \forall X15. \forall X16. \\
& \forall X17. \forall X18. \forall X19. \forall X20. \forall X21. \\
& \forall X22. \neg(\neg(\neg v1_xboole_0 X0) \wedge (v1_xboole_0 (k8_gate_1 (k1_gate_1 \\
& X18) (k1_gate_1 X17) (k1_gate_1 X16)))) \wedge (\neg(\neg v1_xboole_0 (k8_gate_1 \\
& (k1_gate_1 X18) (k1_gate_1 X17) (k1_gate_1 X16))) \wedge (v1_xboole_0 \\
& X0)) \wedge (\neg(\neg v1_xboole_0 X1) \wedge (v1_xboole_0 (k8_gate_1 (k1_gate_1 \\
& X18) (k1_gate_1 X17) X16))) \wedge (\neg(\neg v1_xboole_0 (k8_gate_1 (k1_gate_1 \\
& X18) (k1_gate_1 X17) X16)) \wedge (v1_xboole_0 X1)) \wedge (\neg(\neg v1_xboole_0 \\
& X2) \wedge (v1_xboole_0 (k8_gate_1 (k1_gate_1 X18) X17 (k1_gate_1 X16)))) \wedge \\
& ((\neg(\neg v1_xboole_0 (k8_gate_1 (k1_gate_1 X18) X17 (k1_gate_1 X16))) \wedge \\
& (v1_xboole_0 X2)) \wedge (\neg(\neg v1_xboole_0 X3) \wedge (v1_xboole_0 (k8_gate_1 \\
& (k1_gate_1 X18) X17 X16)))) \wedge (\neg(\neg v1_xboole_0 (k8_gate_1 (k1_gate_1 \\
& X18) X17 X16)) \wedge (v1_xboole_0 X3)) \wedge (\neg(\neg v1_xboole_0 X4) \wedge (v1_xboole_0 \\
& (k8_gate_1 X18 (k1_gate_1 X17) (k1_gate_1 X16)))) \wedge (\neg(\neg v1_xboole_0 \\
& (k8_gate_1 X18 (k1_gate_1 X17) (k1_gate_1 X16))) \wedge (v1_xboole_0 \\
& X4)) \wedge (\neg(\neg v1_xboole_0 X5) \wedge (v1_xboole_0 (k8_gate_1 X18 (k1_gate_1 \\
& X17) X16))) \wedge (\neg(\neg v1_xboole_0 (k8_gate_1 X18 (k1_gate_1 X17) X16)) \wedge \\
& (v1_xboole_0 X5)) \wedge (\neg(\neg v1_xboole_0 X6) \wedge (v1_xboole_0 (k8_gate_1 \\
& X18 X17 (k1_gate_1 X16)))) \wedge (\neg(\neg v1_xboole_0 (k8_gate_1 X18 X17 \\
& (k1_gate_1 X16))) \wedge (v1_xboole_0 X6)) \wedge (\neg(\neg v1_xboole_0 X7) \wedge \\
& v1_xboole_0 (k8_gate_1 X18 X17 X16))) \wedge (\neg(\neg v1_xboole_0 (k8_gate_1 \\
& X18 X17 X16)) \wedge (v1_xboole_0 X7)) \wedge (\neg(\neg v1_xboole_0 X8) \wedge (v1_xboole_0 \\
& (k8_gate_1 (k1_gate_1 X21) (k1_gate_1 X20) (k1_gate_1 X19)))) \wedge \\
& ((\neg(\neg v1_xboole_0 (k8_gate_1 (k1_gate_1 X21) (k1_gate_1 X20) (\\
& k1_gate_1 X19)))) \wedge (v1_xboole_0 X8)) \wedge (\neg(\neg v1_xboole_0 X9) \wedge (v1_xboole_0 \\
& (k8_gate_1 (k1_gate_1 X21) (k1_gate_1 X20) X19))) \wedge (\neg(\neg v1_xboole_0 \\
& (k8_gate_1 (k1_gate_1 X21) (k1_gate_1 X20) X19)) \wedge (v1_xboole_0 \\
& X9)) \wedge (\neg(\neg v1_xboole_0 X10) \wedge (v1_xboole_0 (k8_gate_1 (k1_gate_1 \\
& X21) X20 (k1_gate_1 X19)))) \wedge (\neg(\neg v1_xboole_0 (k8_gate_1 (k1_gate_1 \\
& X21) X20 (k1_gate_1 X19)) \wedge (v1_xboole_0 X10)) \wedge (\neg(\neg v1_xboole_0 \\
& X11) \wedge (v1_xboole_0 (k8_gate_1 (k1_gate_1 X21) X20 X19))) \wedge (\neg(\neg \\
& v1_xboole_0 (k8_gate_1 (k1_gate_1 X21) X20 X19)) \wedge (v1_xboole_0 \\
& X11)) \wedge (\neg(\neg v1_xboole_0 X12) \wedge (v1_xboole_0 (k8_gate_1 X21 (k1_gate_1 \\
& X20) (k1_gate_1 X19)))) \wedge (\neg(\neg v1_xboole_0 (k8_gate_1 X21 (k1_gate_1 \\
& X20) (k1_gate_1 X19))) \wedge (v1_xboole_0 X12)) \wedge (\neg(\neg v1_xboole_0 \\
& X13) \wedge (v1_xboole_0 (k8_gate_1 X21 (k1_gate_1 X20) X19))) \wedge (\neg(\neg \\
& v1_xboole_0 (k8_gate_1 X21 (k1_gate_1 X20) X19)) \wedge (v1_xboole_0 \\
& X13)) \wedge (\neg(\neg v1_xboole_0 X14) \wedge (v1_xboole_0 (k8_gate_1 X21 X20 \\
& (k1_gate_1 X19)))) \wedge (\neg(\neg v1_xboole_0 (k8_gate_1 X21 X20 (k1_gate_1 \\
& X19))) \wedge (v1_xboole_0 X14)) \wedge (\neg(\neg v1_xboole_0 X15) \wedge (v1_xboole_0 \\
& (k8_gate_1 X21 X20 X19))) \wedge (\neg(\neg v1_xboole_0 (k8_gate_1 X21 X20 \\
& X19)) \wedge (v1_xboole_0 X15)) \wedge (\neg(\neg v1_xboole_0 X19) \wedge (v1_xboole_0 \\
& (k2_gate_1 (k1_gate_1 X16) X22))) \wedge (\neg(\neg v1_xboole_0 (k2_gate_1 \\
& (k1_gate_1 X16) X22)) \wedge (v1_xboole_0 X19)) \wedge (\neg(\neg v1_xboole_0 (k2_gate_1 \\
& (v1_xboole_0 (k2_gate_1 (k4_gate_1 X16 X17) X22))) \wedge (\neg(\neg v1_xboole_0 \\
& (k2_gate_1 (k4_gate_1 X16 X17) X22)) \wedge (v1_xboole_0 X20)) \wedge (\neg(\neg \\
& v1_xboole_0 X21) \wedge (v1_xboole_0 (k2_gate_1 (k3_gate_1 (k2_gate_1 \\
& X18 (k1_gate_1 X16)) (k2_gate_1 X16 (k4_gate_1 X17 X18))) X22))) \wedge \\
& ((\neg(\neg v1_xboole_0 (k2_gate_1 (k3_gate_1 (k2_gate_1 X18 (k1_gate_1 \\
& X16)) (k2_gate_1 X16 (k4_gate_1 X17 X18))) X22)) \wedge (v1_xboole_0 \\
& X21)) \wedge (\neg(\neg v1_xboole_0 X9) \wedge (v1_xboole_0 (k2_gate_1 X0 X22))) \wedge \\
& ((\neg(\neg v1_xboole_0 (k2_gate_1 X0 X22)) \wedge (v1_xboole_0 X9)) \wedge (\neg(\neg \\
& v1_xboole_0 X10) \wedge (v1_xboole_0 (k2_gate_1 X1 X22))) \wedge (\neg(\neg v1_xboole_0 \\
& (k2_gate_1 X1 X22)) \wedge (v1_xboole_0 X10)) \wedge (\neg(\neg v1_xboole_0 X11) \wedge \\
& (v1_xboole_0 (k2_gate_1 X2 X22))) \wedge (\neg(\neg v1_xboole_0 (k2_gate_1 \\
& X2 X22)) \wedge (v1_xboole_0 X11)) \wedge (\neg(\neg v1_xboole_0 X12) \wedge (v1_xboole_0 \\
& (k2_gate_1 X3 X22))) \wedge (\neg(\neg v1_xboole_0 (k2_gate_1 X3 X22)) \wedge (v1_xboole_0
\end{aligned}$$