t4_gate_4 (TMPFkLek6biowpqRTSS7kaTt7xz6D496hN6)

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Let $v1\_xboole\_0 : \iota \Rightarrow o$ be given. Let $k4\_gate\_1 : \iota \Rightarrow \iota \Rightarrow \iota$ be given. Let $k2\_gate\_1 : \iota \Rightarrow \iota \Rightarrow \iota$ be given. Assume the following.

$$\forall X0.\forall X1.((\neg v1\_xboole\_0\ X0) \wedge (\neg v1\_xboole\_0\ X1)) \Rightarrow (v1\_xboole\_0\ (k4\_gate\_1\ X0\ X1)) \tag{1}$$

Assume the following.

$$\forall X0.\forall X1.((v1\_xboole\_0\ X0) \wedge (v1\_xboole\_0\ X1)) \Rightarrow (v1\_xboole\_0\ (k4\_gate\_1\ X0\ X1)) \tag{2}$$

Assume the following.

$$\forall X0.\forall X1.((v1\_xboole\_0\ X0) \wedge (\neg v1\_xboole\_0\ X1)) \Rightarrow (\neg v1\_xboole\_0\ (k4\_gate\_1\ X0\ X1)) \tag{3}$$

Assume the following.

$$\forall X0.\forall X1.(v1\_xboole\_0\ X0) \Rightarrow (v1\_xboole\_0\ (k2\_gate\_1\ X0\ X1)) \tag{4}$$

Assume the following.

$$\forall X0.\forall X1.((\neg v1\_xboole\_0\ X0) \wedge (\neg v1\_xboole\_0\ X1)) \Rightarrow (\neg v1\_xboole\_0\ (k2\_gate\_1\ X0\ X1)) \tag{5}$$

Assume the following.

$$\forall X0.\forall X1.k4\_gate\_1\ X0\ X1 = k4\_gate\_1\ X1\ X0 \tag{6}$$

Assume the following.

$$\forall X0.\forall X1.k2\_gate\_1\ X0\ X1 = k2\_gate\_1\ X1\ X0 \tag{7}$$

Theorem 1

$$\forall X0.\forall X1.\forall X2.\forall X3.\forall X4.\forall X5.\ \forall X6.\forall X7.\forall X8.\forall X9.\forall X10.\forall X11.\ \forall X12.\forall X13.\forall X14.\forall X15.\forall X16.\ \forall X17.\forall X18.\forall X19.\forall X20.\forall X21.\ \forall X22.\forall X23.\forall X24.\forall X25.\forall X26.\ \forall X27.\forall X28.\forall X29.\forall X30.\forall X31.\ \forall X32.\forall X33.\forall X34.\forall X35.\forall X36.\ \forall X37.\forall X38.\forall X39.\forall X40.\forall X41.\ \forall X42.\forall X43.\forall X44.\forall X45.\forall X46.\ \forall X47.\forall X48.\forall X49.\forall X50.(v1\_xboole\_0\ X49)\Rightarrow((v1\_xboole\_0\ X0)\vee(((\neg v1\_xboole\_0\ X33)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X50\ X32)))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X50\ X32))\wedge(v1\_xboole\_0\ X33))\vee(((\neg v1\_xboole\_0\ X34)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X17\ (k2\_gate\_1\ X1\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X17\ (k2\_gate\_1\ X1\ X33)))\wedge(v1\_xboole\_0\ X34))\vee(((\neg v1\_xboole\_0\ X35)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X18\ (k2\_gate\_1\ X2\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X18\ (k2\_gate\_1\ X2\ X33)))\wedge(v1\_xboole\_0\ X35))\vee(((\neg v1\_xboole\_0\ X36)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X19\ (k2\_gate\_1\ X3\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X19\ (k2\_gate\_1\ X3\ X33)))\wedge(v1\_xboole\_0\ X36))\vee(((\neg v1\_xboole\_0\ X37)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X20\ (k2\_gate\_1\ X4\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X20\ (k2\_gate\_1\ X4\ X33)))\wedge(v1\_xboole\_0\ X37))\vee(((\neg v1\_xboole\_0\ X38)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X21\ (k2\_gate\_1\ X5\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X21\ (k2\_gate\_1\ X5\ X33)))\wedge(v1\_xboole\_0\ X38))\vee(((\neg v1\_xboole\_0\ X39)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X22\ (k2\_gate\_1\ X6\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X22\ (k2\_gate\_1\ X6\ X33)))\wedge(v1\_xboole\_0\ X39))\vee(((\neg v1\_xboole\_0\ X40)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X23\ (k2\_gate\_1\ X7\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X23\ (k2\_gate\_1\ X7\ X33)))\wedge(v1\_xboole\_0\ X40))\vee(((\neg v1\_xboole\_0\ X41)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X24\ (k2\_gate\_1\ X8\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X24\ (k2\_gate\_1\ X8\ X33)))\wedge(v1\_xboole\_0\ X41))\vee(((\neg v1\_xboole\_0\ X42)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X25\ (k2\_gate\_1\ X9\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X25\ (k2\_gate\_1\ X9\ X33)))\wedge(v1\_xboole\_0\ X42))\vee(((\neg v1\_xboole\_0\ X43)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X26\ (k2\_gate\_1\ X10\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X26\ (k2\_gate\_1\ X10\ X33)))\wedge(v1\_xboole\_0\ X43))\vee(((\neg v1\_xboole\_0\ X44)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X27\ (k2\_gate\_1\ X11\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X27\ (k2\_gate\_1\ X11\ X33)))\wedge(v1\_xboole\_0\ X44))\vee(((\neg v1\_xboole\_0\ X45)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X28\ (k2\_gate\_1\ X12\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X28\ (k2\_gate\_1\ X12\ X33)))\wedge(v1\_xboole\_0\ X45))\vee(((\neg v1\_xboole\_0\ X46)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X29\ (k2\_gate\_1\ X13\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X29\ (k2\_gate\_1\ X13\ X33)))\wedge(v1\_xboole\_0\ X46))\vee(((\neg v1\_xboole\_0\ X47)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X30\ (k2\_gate\_1\ X14\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X30\ (k2\_gate\_1\ X14\ X33)))\wedge(v1\_xboole\_0\ X47))\vee(((\neg v1\_xboole\_0\ X48)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ X31\ (k2\_gate\_1\ X15\ X33))))\vee(((\neg v1\_xboole\_0\ (k4\_gate\_1\ X31\ (k2\_gate\_1\ X15\ X33)))\wedge(v1\_xboole\_0\ X48))\vee((\neg(\neg v1\_xboole\_0\ X48)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ (k4\_gate\_1\ X31\ (k2\_gate\_1\ X15\ X32))\ (k4\_gate\_1\ X49\ (k2\_gate\_1\ X15\ X50)))))\wedge((\neg(\neg v1\_xboole\_0\ (k4\_gate\_1\ (k4\_gate\_1\ X31\ (k2\_gate\_1\ X15\ X32))\ (k4\_gate\_1\ X49\ (k2\_gate\_1\ X15\ X50))))\wedge(v1\_xboole\_0\ X48))\wedge((\neg(\neg v1\_xboole\_0\ X47)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ (k4\_gate\_1\ X30\ (k2\_gate\_1\ X14\ X32))\ (k4\_gate\_1\ X49\ (k2\_gate\_1\ X14\ X50)))))\wedge((\neg(\neg v1\_xboole\_0\ (k4\_gate\_1\ (k4\_gate\_1\ X30\ (k2\_gate\_1\ X14\ X32))\ (k4\_gate\_1\ X49\ (k2\_gate\_1\ X14\ X50))))\wedge(v1\_xboole\_0\ X47))\wedge((\neg(\neg v1\_xboole\_0\ X46)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ (k4\_gate\_1\ X29\ (k2\_gate\_1\ X13\ X32))\ (k4\_gate\_1\ X49\ (k2\_gate\_1\ X13\ X50)))))\wedge((\neg(\neg v1\_xboole\_0\ (k4\_gate\_1\ (k4\_gate\_1\ X29\ (k2\_gate\_1\ X13\ X32))\ (k4\_gate\_1\ X49\ (k2\_gate\_1\ X13\ X50))))\wedge(v1\_xboole\_0\ X46))\wedge((\neg(\neg v1\_xboole\_0\ X45)\wedge(v1\_xboole\_0\ (k4\_gate\_1\ (k4\_gate\_1\ X28\ (k2\_gate\_1\ X12\ X32))\ (k4\_gate\_1\ X49\ (k2\_gate\_1\ X12\ X50)))))\wedge((\neg(\neg v1\_xboole\_0\ (k4\_gate\_1\ (k4\_gate\_1\ X28\ (k2\_gate\_1\ X12\ X32))\ (k4\_gate\_1\ X49\ (k2\_gate\_1\ X12\ X50))))\wedge$$